JEAN-LUC GAUDIOT
Distinguished Professor
Department of Electrical Engineering and Computer Science
University of California
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Research Interests

- Programmability of large-scale multiprocessors, distributed structure representation, data caching and nomadic threads, high-level parallel language compilation, allocation, partitioning, and performance evaluation

- Processor architecture, implementation and impact of future technologies

- Fault-tolerant computing, Benchmarking and characterization of applications, design of flexible architectures tuned for specific types of applications

- Design of Autonomous Vehicle Systems

Education

- *Ph.D. in Computer Science* (October 1982), *University of California, Los Angeles*

- *M.Sc. in Computer Science* (June 1977), *University of California, Los Angeles*

- *"Diplôme d'Ingénieur" (Electrical Engineering Diploma)* (June 1976), *École Supérieure d'Ingénieurs en Electronique et Electrotechnique, Paris, France*

Experience

- *PROFESSOR - University of California, Department of Electrical Engineering and Computer Science,* Irvine, California (Since January 2002 - Chair from January 2003 to September 2009)

- *PROFESSOR - University of Southern California, Department of Electrical Engineering-Systems,* Los Angeles, California (August 1996 - December 2001)

- *ASSOCIATE PROFESSOR - University of Southern California, Department of Electrical Engineering-Systems,* Los Angeles, California (June 1989 - August 1996)

- *ASSISTANT PROFESSOR - University of Southern California, Department of Electrical Engineering-Systems,* Los Angeles, California (December 1982 - June 1989)

- *MEMBER OF TECHNICAL STAFF, TRW Technology Research Center*, El Segundo, California (August 1980 - November 1982)

- *SOFTWARE ENGINEER, Teledyne Controls*, Santa Monica, California (March 1979 - August 1980) N23

Awards and Professional Societies Membership

- IEEE CS TCPP Outstanding Service Award (June 2017)

- 2017 IEEE Computer Society President, Elected by the membership, January 1, 2017

- IEEE Eta Kappa Nu, Honor Society of IEEE, Professional Member (inducted December 11, 2015)

- AAAS Fellow (American Association for the Advancement of Science) *"For Distinguished Contributions to the Design and Analysis of Highly Efficient Multiprocessor and Memory System Architectures,"* (October 2007)

- International Federation for Information Processing (IFIP) Silver Core Member *"For Dedication to Outstanding Scientific Work on One Hand and Enormous Service Work on the Other One,"* (September 2007)

- IEEE Computer Society Golden Core Member *"As One of the Distinguished Core of Dedicated Volunteers and Staff whose Leadership and Service have made the IEEE Computer Society the World's Preeminent Association of Computing Professionals,"* (June 2003)

- IEEE Computer Society Meritorious Service Award *"For Outstanding Service as Editor-in-Chief of the IEEE Transactions on Computers,"* (November 2002)

- IEEE Fellow *"For Contributions to the Programmability and Reliability of Dataflow Architectures,"* (January 1999)

- IEEE Computer Society Distinguished Visitor (1994-1998)

- IEEE, IEEE Computer Society, ACM, ACM Sigarch

- IFIP Working Group 10.3 - Concurrent Systems (chair from 1995 to 2001)

- IEEE Computer Society Technical Committee on Computer Architecture (elected chair in June 2001, re-elected in June 2003 - two year terms)

- IEEE Computer Society Technical Committee on Parallel Processing (member of the Advisory Board)

Long-term consulting affiliations

- Northrop Grumman Corporation, Pico Rivera, California (1997-2007)

- Alshuler, Grossman, Stein, and Kahan LLP, Los Angeles, California (2002-2004)

- Language Systems, Inc., Canoga Park, California (1990-1997)

- TRW ESG, Redondo Beach, California (1986-1987)

- Research & Development Associates, Marina Del Rey, California (1985)

- Hughes Aircraft Co, Electro-Optical Systems Division, El Segundo, California (1983-1984)

- Logabax, Los Angeles, California (1978-1979)

Extramural Funding

- Fine-Grain Multithreading through Hardware/Software Co- Design (NSF - shared with the University of Delaware).
  Duration of the award: 3 years (July 2018 through June 2021)
  Amount of the award: $337K)

- SPARTA: a Stream-based Processor And Run-Time Architecture (NSF - shared with the University of Delaware and the University of Arizona).
  Duration of the award: 3 years (July 2014 through June 2017)
  Amount of the award: $271K for UCI (total: $850K)

- Architecture, Programmability and Performance of Large Scale Parallel Systems (NSF - Supplemental funding).
  Duration of the award: 1 year (June 2012 through May 2013)
  Amount of the award: $40K

- Architecture, Programmability and Performance of Large Scale Parallel Systems (NSF - evenly shared with the University of Delaware).
  Duration of the award: 4 years (July 2011 through June 2015)
  Amount of the award: $400K for UCI (total: $800K)

- Exploring Transactional Memory Systems for the Intel SCC (Intel).
  No monetary award; access to the SCC site

- A Flexible, Efficient, and Dynamic Architecture and Compilation Framework for Networking Applications (NSF - Supplemental funding).
  Duration of the award: 1 year (September 2010 through August 2011)
  Amount of the award: $40K

- A Flexible, Efficient, and Dynamic Architecture and Compilation Framework for Networking Applications (NSF - Supplemental funding).
  Duration of the award: 1 year (September 2009 through August 2010)
  Amount of the award: $40K

- DUDECRONO - Dual degree on MicroNanotechnology (Department of Education).
  Date of the Award: August 2009 (4 years)
  Amount of the award: $420K

- A Flexible, Efficient, and Dynamic Architecture and Compilation Framework for Networking Applications (NSF - with a subcontract to the University of Delaware).
  Duration of the award: 3 years (August 2005 through July 2008)
  Amount of the award: $400K

- MRI: HIPerWall: Development of a High-Performance Visualization System for Collaborative Earth System Sciences (NSF).
  Date of the award: August 2004
  Amount of the award: $394K (with F. Kuester, S. Jenks, C. Zender, and S. Sorooshian)

- Application-Specific PIM (Processor-In-Memory) Architecture for Embedded Systems (Microsoft Research).
  Date of the award: August 2003
  Amount of the award: $15K

- Postdoctoral grant (UC Mexus - the University of California Institute for Mexico and the United States).

Duration of the award: 1 year (September 2003 - August 2004)
Amount of the award: $31K

- Parallel Processing and Computer Architecture Workshop (UC Conference and Research Workshop Program). March 2002 ($1,000 with Dr. Stephen Jenks)

- ITR: A Completely Integrated Processor-Memory-Interconnect Architecture Model for Data Intensive Applications (NSF - subcontract from USC).
  Duration of the award: 3 years (August 2002 through July 2005)
  Total amount of the award: $200K (with Prof. Sandeep Gupta at USC)

- E-textiles for Inflatable Systems (DARPA - with JPL. Selected but not funded: program canceled prior to appropriation (February 2002)

- Power Aware Architectures (DARPA - subcontract from UCI).
  Duration of the award: 3 years (August 2000 through July 2003)
  Amount of the award: $150K

- Multithreading - A Viable Approach for High Performance Single-Chip Architectures (NSF - with a subcontract to the University of Delaware).
  Duration of the award: 3 years (August 2000 through July 2003 - extended through July 2004)
  Amount of the award: $600K

- ILP vs. TLP: A Viable Trade-off? (NSF - with a subcontract to the University of Delaware).
  International Program Division: 3 years (June 1999 through May 2002 - extended through July 2004)
  Amount of the award: $20K

- Processor Architectures for DSP Applications (Conexant).
  Date of the award: October 2000
  Amount of the award: $33K

- A Hierarchical Decoupled Instruction Set Computer (DARPA).
  Duration of the award: 3 years (August 1998 through July 2001)
  Amount of the award: $600K (with Al Despain)

- Processor Architectures for DSP Applications (Conexant).
  Date of the award: October 1999)
  Amount of the award: $33K

- Processor Architectures for DSP Applications (Conexant).
  Date of the award: October 1998
  Amount of the award: $33K

- Processor Architectures for DSP Applications (Rockwell Semiconductor Systems).
  Duration of the award: 1 year (October 1997 through September 1998)
  Amount of the award: $33K

- New Generation Multithreaded Multiprocessors (NSF - with a subcontract to the University of Delaware).
  Duration of the award: 3 years (August 1997 through July 2000)
  Amount of the award: $400K

- Formal specification and transformation of parallel programs (NSF).
  International Program Division: 3 years (June 1997 through May 2000)
  Amount of the award: $12K

- An evaluation of high-performance functional computing (DARPA).
  Duration of the award: 3 years (September 1995 to August 1998)
  Amount of the award: $1.2M

- A comparative study of the programmability of a signal processing application in an MIMD and an SIMD multiprocessor (Teledyne Systems Company).
  Amount of the award: $30K (sole PI - March 1994)

- Equipment for research in designing and using multiprocessor systems (NSF) with A. Despain (May 1992).
  Amount of the award: $85K

- A study of genetic programming for infra-red image analysis (Hughes Aircraft).
  Amount of the award: $30K (sole PI - December 1993)

- Programming and evaluating the performance of signal processing applications in a parallel environment (Teledyne Systems Company).
  Amount of the award: $30K (sole PI - March 1991)

- Programming parallel machines for knowledge-based applications (Language Systems, Inc.).
  Duration of the award: 1.5 years (November 1991 to January 1993)
  Amount of the award: $27K
  Level of support: 1 Research Assistant (sole PI)

- A data-driven approach to programming multiprocessor systems (National Science Foundation).
  Duration of the award: 2 years (March 1991 to March 1993)
  Amount of the award: $171K
  Level of support: 2 summer months, 1.5 Research Assistant (sole PI)

- Neurobiology and simulation of neural nets for invariant object recognition (Air Force Office of Scientific Research with C. von der Malsburg and E. Rolls).
  Duration of the award: 3 years (May 1988 to May 1991).
  Amount of the award: $600K
  Level of support: 10% academic year, 1 Research Assistant

- A multi-level data-flow architecture for signal and data processing applications (Department of Energy, Office of Energy Research).
  Duration of the award: 4 years (May 1987 to July 1991)
  Amount of the award: $603K
  Level of support: 40% academic year, 1 summer month, 3 Research Assistants (sole PI)

- Research on architectural issues in data-flow multicomputers (NSF).
  Duration of the award: 3 years (May 1987 to June 1990)
  Amount of the award: $171K
  Level of support: 2 summer months, 1.5 Research Assistant (sole PI)

- Research in Computer Architecture (NSF) with M. Dubois and K. Hwang (June 1986).
  Amount of the award: $56K

- Logic programming in data-flow systems (USC Faculty Research and Innovation Fund).
  Duration of the award: 1 year (June 86 to May 87)
  Amount of the award: $18K (sole PI)

- Survey of simulation languages (Rockwell International).
  Duration of the award: 1 month (August 1985).
  Amount of the award: $5K (sole PI)

- Performance analysis of a reconfigurable multiprocessor system (USC Faculty Research and Innovation Fund with M. Dubois).
  Duration of the award: 1 year (June 85 to May 86).
  Amount of the award: $18.5K

- Variable resolution in data-flow systems (NSF Initiation Grant).
  Duration of the award: 2 years (June 84 to May 86).
  Amount of the award: $48K (sole PI)

- Performance evaluation of data-flow multiprocessors (USC Faculty Research and Initiation Fund).
  Duration of the award: 1 year (June 84 to May 85).
  Amount of the award: $8K (sole PI)

Books

[B6] S. Liu, L. Li, J. Tang, S. Wu, and J-L. Gaudiot, *Creating Autonomous Vehicle Systems*, ISBN: 9781681730073 — PDF ISBN: 9781681730080, Morgan & Claypool Publishers, August 2017.

[B5] L. Bic, W. Böhm, P. Evripidou, and J-L. Gaudiot (Eds.), *Proceedings of the IFIP WG 10.3 Working Conference on Parallel Architectures and Compilation Techniques, PACT '95*, ACM Press, June 27-29, 1995.

[B4] G.R. Gao, L. Bic, and J-L. Gaudiot (Eds.), *Advanced topics in dataflow computing and multithreading,* IEEE Computer Society Press, 1995.

[B3] M. Cosnard, K. Ebcioğlu, and J-L. Gaudiot. (Eds.), *Proceedings of the IFIP WG10.3 Working Conference on Architectures and Compilation Techniques for Fine and Medium Grain Parallelism,* IFIP Transactions, North Holland, 1993.

[B2] D. Abramson and J-L. Gaudiot. (Eds.), *Proceedings of the Nineteenth Annual International Symposium on Computer Architecture,* ACM Press, 1992.

[B1] J-L. Gaudiot and L. Bic. (Eds.), *Advanced Topics in Data-Flow Computing*, Prentice Hall, 1991.

Books chapters and reprints

[BC18] C. Liu, X. Li, S. Liu and J-L. Gaudiot, "Simultaneous MultiThreading Microarchitecture," in *Handbook of Research on Scalable Computing Technologies, edited by Kuan-Ching Li, Ching-Hsien Hsu, Laurence T. Yang, Jack Dongarra, Hans Zima*, IGI Global, pp. 552–582, 2009.

[BC17] J-L. Gaudiot, J-Y. Kang, and W.W. Ro, "Improving performance beyond pipelining: superpipelining, superscalar and VLIW," in *Computer Architecture, (a volume of Advances in Computers), edited by Ali R. Hurson*, Elsevier, Inc., 2004.

[BC16] C. Shin, S.W. Lee, and J-L. Gaudiot, "The need for adaptive dynamic thread scheduling," in *High Performance Scientific and Engineering Computing - Hardware/Software Support, edited by L.T. Yang and Y. Pan*, Kluwer Publishing, 2004.

[BC15] J-L. Gaudiot, "Foreword," in *Parallel I/O for Cluster Computing, by C. Cérin and Hai Jin*, Kluwer Publishing, 2002

[BC14] J-L. Gaudiot, "Préface," in *Architecture et micro-architecture des processeurs, Springer-France by Bernard Goossens*, 2002 (in French).

[BC13] J-L. Gaudiot, "Introduction to computer architecture and design," chapter in *Computer Engineering Handbook,* January 2002.

[BC12] S. Shams and J-L. Gaudiot, "Regularly structured neural networks on the DREAM machine," chapter 9 in *Parallel Architectures for Artificial Neural Networks, Paradigms and Implementations,* IEEE Computer Society, N. Sundararajan and P. Saratchansdran, Eds., 1998.

[BC11] C. Kim and J-L. Gaudiot, "Data-flow and multithreaded architectures," chapter in *Encyclopedia of Electrical and Electronics Engineering,* Wiley Pub., May 1997.

[BC10] J-L. Gaudiot, T. DeBoni, J. Feo, W. Böhm, and P. Miller, "The Sisal project: real world functional computing," chapter 2 in *Languages, Compilation Techniques and Run Time Systems for Scalable Parallel Systems, Recent Advances and Future Perspectives,* Springer Verlag Lecture Notes in Computer Science Series, 1997.

[BC9] J-L. Gaudiot and A. Sohn, "Programmability and Performance Issues of Multiprocessors on Hard Nonnumeric Problems," chapter in *Advanced topics in dataflow computing and multithreading,* IEEE Computer Society Press, 1995.

[BC8] J-L. Gaudiot and C. Kim, "Data-driven and multithreaded architectures for high-performance computing," chapter in *Parallel Computers, Theory and Practice*, pp. 73-105, IEEE Computer Society Press, 1996.

[BC7] A. Sohn and J-L. Gaudiot, "Connectionist production systems in local and hierarchical representation," chapter in *Applications of Learning and Planning Methods,* World Scientific Publishing Co., N.G. Bourbakis, Ed., 1991.

[BC6] J-L. Gaudiot and D.K. Yoon, "Occam," chapter in *A Comparative Study of Parallel Programming Languages: The Salishan Problems,* Special Topics in Supercomputing, Vol.6, pp.217-262, North Holland, Amsterdam, The Netherlands, John Feo, Ed., 1992.

[BC5] P. Evripidou and J-L. Gaudiot, "The USC Decoupled Multilevel Data-Flow Execution Model," chapter in *Advanced Topics in Data-Flow Computing,* J-L. Gaudiot and L. Bic, eds., Prentice Hall, 1990.

[BC4] W. Najjar and J-L. Gaudiot, "Macro data-flow architectures," chapter in *Dataflow Computing: Theory and Practice,* Ablex Publishing, John Sharp, Ed., 1992.

[BC3] J-L. Gaudiot and L. Bic, "Data-Flow: A Status Report," unrefereed article in *ACM SIGARCH Computer Architecture News,* Vol. 17, No. 6, pp. 111-118, December 1989.

[BC2] J-L. Gaudiot, "Data-flow machines," chapter in *Topics in High-Level Language Computer Architecture,* Computer Science Press, V. Milutinovic, Ed., August 1988.

[BC1] J-L. Gaudiot, M. Dubois, L.T. Lee, and N. Tohmé, "The TX16: A highly programmable multiprocessor architecture," reprinted in *Multi-Microprocessors*, IEEE Press, A. Gupta, ed., 1987 (originally published in *IEEE Micro*, October 1986).

Journal Publications

[J93] S. Liu, J. Tang, C. Wang, Q. Wang, and J-L. Gaudiot, "Implementing a Cloud Platform for Autonomous Driving," *IEEE Computer,* Volume 50, Issue 12, ISSN: 0018-9162, pp. 42-49 DOI: http://doi.ieeecomputersociety.org/10.1109/MC.2017.4451224, November 2017.

[J92] J. Tang, D. Sun, S. Liu, , and J-L. Gaudiot, "Enabling Deep Learning on IoT Devices," *IEEE Computer,* Volume 50, Issue 10, pp. 92-96, DOI: 10.1109/MC.2017.3641648, October 2017.

[J91] S. Liu, J. Tang, Z. Zhang, and J-L. Gaudiot, "Computer Architecture for Autonomous Driving," *IEEE Computer,* Volume 50, Issue 8, pp. 18-25, DOI: 10.1109/MC.2017.3001256, August 2017.

[J90] J-Y. Young, T-H. You, H. Seo, S. Yoon, J-L. Gaudiot, and E-Y. Young "An effective pre-store/pre-load method exploiting intra-request idle time of NAND flash-based storage devices," *Microprocessors and Microsystems,* Volume 50, pp. 222236, May 2017.

[J89] S. Pei, J. Zhang, N. Xiong, M-S. Kim, and J-L. Gaudiot, "Energy Efficiency of Heterogeneous Multicore System Based on the Enhanced Amdahls Law," *Int. J. High Performance Computing and Networking,* August 2016.

[J88] S. Pei, M-S. Kim, and J-L. Gaudiot, "Extending Amdahl's Law for Heterogeneous Multicore Processor with Consideration of the Overhead of Data Preparation," *IEEE Embedded Systems Letters,* DOI: 10.1109/LES.2016.2519521, March 2016.

[J87] S. Pei, J. Zhang, L. Jiang, M-S. Kim and J-L. Gaudiot, "Reevaluating the overhead of data preparation for asymmetric multicore system on graphics processing", *KSII Transactions on Internet and Information Systems*, vol. 10, no. 7, pp. 3231-3244, July 2016. DOI: 10.3837/tiis.2016.07.020

[J86] K. Kim, B.Y. Cho, W.W. Ro, and J-L. Gaudiot, "Network Variation and Fault Tolerant Performance Acceleration in Mobile Devices with Simultaneous Remote Execution," *IEEE Transactions on Computers*, DOI: 10.1109/TC.2015.2389809, Volume 64, Issue 10, pp. 2662-2874, October 2015.

[J85] S.H. Kim, D. Kim, C. Lee, W.S. Jeong, W.W. Ro, and J-L. Gaudiot, "A Performance-Energy Model to Evaluate Single Thread Execution Acceleration," *Computer Architecture Letters*, DOI: 10.1109/LCA.2014.2368144, Volume 13, Number 2, pp. 99-102, July-December 2015.

[J84] Y-L. Chou, S. Liu, E-Y. Chung, and J-L. Gaudiot, "An Energy and Performance Efficient DVFS Scheme for Irregular Parallel Divide-and-Conquer Algorithms on the Intel SCC," *Computer Architecture Letters*, DOI: 10.1109/L-CA.2013.1, Volume 13, Number 1, pp 13-16, January-June 2014.

[J83] S.H. Kim, S.H. Lee, M. Jun, B. Lee, W.W. Ro, E.-Y. Chung, and J-L. Gaudiot, "C-Lock: Energy Efficient Synchronization for Embedded Multicore Systems," *IEEE Transactions on Computers*, DOI: 10.1109/TC.2013.84, Volume 63, No. 8, Pages 1962–1974, August 2014.

[J82] C. Liu, P. Thanarungroj, and J-L.Gaudiot, "How Many Cores We Need to Run a Parallel Workload? A Test Drive of the Intel SCC Platform," *Journal of Parallel and Distributed Computing*, http://dx.doi.org/10.1016/j.jpdc.2013.12.011, Volume 74, Issue 7, Pages 2582?-2595, July 2014.

[J81] S.H. Kim, D. Choi, W.W. Ro, and J-L. Gaudiot, "Complexity-Effective Contention Management with Dynamic Backoff for Transactional Memory Systems," *IEEE Transactions on Computers*, DOI: 10.1109/TC.2013.49, Volume 63, Number 7, Pages 1696–1708, July 2014.

[J80] H. Jiang, Y. Chen, Z. Qiao, K-C. Li, W. Ro, and J-L. Gaudiot, "Accelerating MapReduce Framework on Multi-GPU Systems," *Cluster Computing*, DOI: 10.1007/s10586-013-0276-5, Volume 17, Issue 2, Pages 293–301, June 2014.

[J79] C. Lee, W.W. Ro, and J-L. Gaudiot, "Boosting CUDA Applications with CPU – GPU Hybrid Computing," *International Journal of Parallel Programming*, DOI: 10.1007/s10766-013-0252-y, Volume 42, Issue 2, Pages 384–404, April 2014.

[J78] J. Tang, C. Liu, S. Liu, and J-L. Gaudiot, "Practical models for energy-efficient prefetching in mobile embedded systems," *Microprocessors and Microsystems*," DOI: 10.1016/j.micpro.2013.09.004, Volume 37, Issue 8, Part D, Pages 1173–1182, November 2013.

[J77] M. Mehri Dehnavi, D. Fernandez, J-L. Gaudiot, and D. Giannacopoulos, "Parallel Sparse Approximate Inverse Preconditioning on Graphic Processing Units," *IEEE Transactions on Parallel and Distributed Systems*, DOI: 10.1109/TPDS.2012.286, Volume 24, Issue 9, Pages 1852 – 1862, September 2013.

[J76] J. Tang, S. Liu, C. Liu, and J-L. Gaudiot, "Acceleration of XML Parsing Through Prefetching," *IEEE Transactions on Computers*, DOI: 10.1109/TC.2012.88, Volume 62, Issue 8, Pages 1616–1628, August 2013.

[J75] S. Kim, W.S. Jeong, W.W. Ro, and J-L. Gaudiot, "Design and Evaluation of Random Linear Network Coding Accelerators on FPGAs," *ACM Transactions on Embedded Computing Systems*, DOI: 10.1145/2512469, Volume 13, Issue 1, August 2013.

[J74] M-S. Kim, C. G. Kim, S.D. Kim, and J-L. Gaudiot, "Design of configurable I/O pin control block for improving reusability in multimedia SoC platforms," *International Journal of Multimedia Tools and Applications*, DOI: 10.1007/s11042-013-1598-2, July 2013.

[J73] S. Liu, R. Pittman, A. Forin, and J-L. Gaudiot, "Achieving Energy Efficiency through Run-Time Partial Reconfiguration on Reconfigurable Systems," *ACM Transactions on Embedded Computing Systems*, DOI: 10.1145/2442116.2442122, Volume 12, Issue 3, March 2013.

[J72] J. Tang, P. Thanarungroj, C. Liu, S. Liu, Z. Gu, and J-L. Gaudiot, "Pinned OS/Services: A Case Study of XML Parsing on Intel SCC," *Journal of Computer Science and Technology*, DOI: 10.1007/s11390-013-1308-6, Volume 28, Issue 1, Pages 3–13, January 2013.

[J71] K. Yi, W. Ro, and J-L. Gaudiot, "Importance of Coherence Protocols with Network Applications on Multi-Core Processors," *IEEE Transactions on Computers*, Volume: 62, Issue: 1, DOI: 10.1109 / TC.2011.199, Volume 62, Issue 1, Pages 6–15, January 2013.

[J70] S. Liu, W. W. Ro, C. Liu, A.C. Salas, C. Cérin, J-J. Han, and J-L. Gaudiot, "Introducing the Extremely Heterogeneous Architecture," *Journal of Interconnection Networks*, Volume 13, Issue 03-04, September & December 2012.

[J69] J.J. Han, X. Wu, D. Zhu, H. Jin, L. Yang, and J-L. Gaudiot, "Synchronization-Aware Energy Management for VFI-based Multicore Real-Time Systems," *IEEE Transactions on Computers*, DOI: 10.1109/TC.2012.136, Volume 61 , Issue 12, Pages 1682–1696, December 2012.

[J68] S. Liu, J. Tang, L. Wang, X-F. Li, and J-L. Gaudiot, "Packer: Parallel Garbage Collection Based on Virtual Spaces," *IEEE Transactions on Computers*, DOI: 10.1109 / TC.2011.193, Volume 61, Issue 11, Pages 1611–1623, November 2012.

[J67] S. Liu, R.N. Pittman, A. Forin, and J-L. Gaudiot, "Minimizing the Runtime Partial Reconfiguration Overheads in Reconfigurable Systems," *Journal of Supercomputing*, DOI: 10.1007 / s11227-011-0657-6, Volume 61, Issue 3, Pages 894-911, July 2011.

[J66] J. Tang, S. Liu, C. Liu, Z. Gu, and J-L. Gaudiot, "Prefetching in Embedded Mobile Systems Can Be Energy-Efficient," *Computer Architecture Letters*, DOI: 10.1109/L-CA.2011.2, Volume 10, Number 1, Pages 8–11, January-June 2011.

[J65] S. Liu, C. Eisenbeis, and J-L. Gaudiot, "Value Prediction and Speculative Execution on GPU," *International Journal of Parallel Programming*, DOI: 10.1007/s10766-010-0155-0, Volume 39, Issue 5, Pages 533–552, October 2011.

[J64] J. Tang, S. Liu, Z. Gu, X-F. Li, and J-L. Gaudiot, "Achieving Middleware Execution Efficiency: Hardware-Assisted Garbage Collection Operations," *Journal of Supercomputing*, DOI: 10.1007/s11227-010-0493-0, Volume 59, Issue 3, Pages 1101-1119, March 2012.

[J63] S. Liu, X-F. Li, L. Wang, and J-L. Gaudiot, "Space-and-Time Efficient Parallel Garbage Collector for Data-Intensive Applications," *International Journal of Parallel Programming*, DOI:10.1007/s10766-010-0151-4, Volume 39, Issue 4, Pages 451–472, August 2011.

[J62] H. Homayoun, A. Veidenbaum, A. Sasan, and J-L. Gaudiot, "Reducing Power in All Major CAM and SRAM Based Processor Units via Centralized, Dynamic Resource Size Management," *IEEE Transactions on Very Large Scale Integration Systems*, DOI: 10.1109 / TVLSI.2010.2064185, Volume 19, Issue 11, Pages 2081–2094, November 2011.

[J61] K. Yi and J-L. Gaudiot, "Network Applications on Simultaneous MultiThreading Processors," *IEEE Transactions on Computers*, DOI:10.1109TC.209.185, Volume 59, Issue 9, Pages 1200-1209, September 2010.

[J60] S. Liu, J. Tang, C. Deng, X-F. Li, and J-L. Gaudiot, "RHE: A JVM Courseware," *IEEE Transactions on Education*, Issue: 99, DOI: 10.1109/TE.2010.2047946, Volume 54, Issue 1, Pages 141–148, February 2011.

[J59] X. Li and J-L. Gaudiot, "Tolerating Radiation-Induced Transient Faults in Modern Processors," *International Journal of Parallel Programming*, ISSN 0885-7458 (Print) 1573-7640 (Online), DOI:10.1007/s10766-009-0114-9, Volume 38, Issue 2, Page 85–116, April 2010.

[J58] S. Liu and J-L. Gaudiot, "Potential Impact of Value Prediction on Communication in Many-Core Architectures," *IEEE Transactions on Computers*, DOI:10.1109/TC.2009.28, Volume 58, No. 6, Pages 759–769, June 2009.

[J57] W.W. Ro and J-L. Gaudiot, "A Complexity-Effective Microprocessor Design with Decoupled Dispatch Queues and Prefetching," *Parallel Computing*, DOI:10.1016/j.parco.2008.12.008, Volume 35, Issue 5, Pages 255–268, May 2009.

[J56] W.W. Ro and J-L. Gaudiot, "A Low-Complexity Microprocessor Design with Speculative Pre-Execution," *Journal of Systems Architecture*, DOI:10.1016/j.sysarc.2008.05.003, Volume 54, Issue 12, Pages 1101-1112, December 2008.

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[C7]   J-L. Gaudiot and M. Dubois, "An integrated solution to large-scale computing problems," in *Proceedings of the International Symposium on New Directions in Computing*, Trondheim, Norway, August 1985.

[C6]   J-L. Gaudiot, "Methods for handling structures in data-flow systems," in *Proceedings of the Twelfth Annual Symposium on Computer Architecture (ISCA)*, pp. 352-258, Boston, Massachusetts, June 1985.

[C5]   J-L. Gaudiot and C. S. Raghavendra, "Fault-tolerance and data-flow systems," in *Proceedings of the Fifth International Conference on Distributed Computing Systems (ICDSC)*, pp. 16-23, Denver, Colorado, May 1985.

[C4]   J-L. Gaudiot and M.D. Ercegovac, "Performance Analysis of a Data-Flow Computer with Variable Resolution Actors," in *Proceedings of the Fourth International Conference on Distributed Computing Systems (ICDSC)*, pp. 2-9, San Francisco, California, May 1984.

[C3]   J-L. Gaudiot and M.D. Ercegovac, "Evaluation of ring communication networks in a data-flow computer," in *Proceedings of the Third Annual Phoenix Conference on Computers and Communications*, Phoenix, Arizona, March 1984.

[C2]   J-L. Gaudiot and M.D. Ercegovac, "Simulation of a data-flow machine using the SARA system," in *Proceedings of the Seventeenth Asilomar Conference on Circuits, Systems and Computers*, pp. 485-489, Monterey, California, October 1983.

[C1]   J-L. Gaudiot and M.D. Ercegovac, "A scheme for handling arrays in data-flow systems," in *Proceedings of the Third International Conference on Distributed Computing Systems*, pp. 724-729, Fort Lauderdale, Florida, October 1982.

Other Publications

[N47]   J-L. Gaudiot, Embracing changes, *Computer*, December 2017.

[N46]   S. Liu, J. Peng, and J-L. Gaudiot, Computer, Drive my car!, *IEEE Computer*, Volume 50, Issue 1, pp.8-8, January 2017.

[N45]   J-L. Gaudiot, The New Computer Society, *Computer*, January 2017.

[N44]   A. Banifatemi and J-L. Gaudiot, Engineering the New Boundaries of AI, *IEEE Computer*, December 2016.

[N43]   J-L. Gaudiot, Introduction to *The Researcher,* section in *Computing Now*, August 2016

[N42]   J-L. Gaudiot, Endorsement for *Encyclopedia of Cloud Computing*, San Murugesan and Irena Bojanova, published by Wiley and IEEE, 2016

[N41]   J-L. Gaudiot, "The Times They Are A-Changin', so let's get in front of these changes! A report on the state of the Publications Board," *Computer*, June 2015

[N40]   G. Araújo, J-L. Gaudiot, M. Parashkar, D. Chiou, J.N. Amaral, and C.R. Das, "Guest Editorial," *International Journal on Parallel Programming - Special Issue on Computer Architecture* (2015) 43:961964 DOI 10.1007/s10766-015-0377-2

[N39] W. W Ro, C. Liu, and J-L. Gaudiot, "Reconfigurability and Power Issues in Computer Systems Design - Guest Editors Introduction," *Computing Now*, November 2014

[N38] J-L. Gaudiot, "IEEE Rebooting Computing Summit," May 2014 (Video)
http://www.computer.org/portal/web/computingnow/events#summit

[N37] J-L. Gaudiot, "Computing Now April Monthly Theme on Semantics in Education," April 2014 (Video)
http://www.computer.org/portal/web/computingnow/archive/april2014

[N36] A. Melo, J-L. Gaudiot, L. DeRose, K. Olukotun, and A. Zomaya, "Guest Editorial," *International Journal on Parallel Programming - Special Issue on Computer Architecture*, DOI: 10.1007/s10766-013-0255-8, Volume 42, Issue 1, pp 1-3, February 2014.

[N35] J-L. Gaudiot, "A MOOC on Software Engineering," December 2013 (Video)
http://www.computer.org/portal/web/certification/courses/MOOC

[N34] P. Evripidou, I. Watson, G.R. Gao, J-L. Gaudiot, and V. Sarkar, "Preface," *2012 Second Workshop on Data-Flow Execution Models for Extreme Scale Computing DFM 2012*, Minneapolis, Minnesota, September 2012.

[N33] J-L. Gaudiot, "Importance of Coherence Protocols with Network Applications on Multi-Core Processors," in *Computing Now*, January 2012 (Video),
http://www.computer.org/portal/web/computingnow/0112/whatsnew/tc

[N32] A. Melo and J-L. Gaudiot, "Word from the Program Chairs," *Symposium on Computer Architecture and High Performance Computing (SBAC-PAD 2011)*, Vitória, Brazil, October 2011.

[N31] J-L. Gaudiot, "TC celebrates its 60th anniversary," *IEEE Transactions on Computers*, Volume 60, Issue 5, May 2011.

[N30] J-L. Gaudiot, "Introducing the New Editor-in-Chief of IEEE Computer Architecture Letters," *IEEE Computer Architecture Letters*, Volume 8, Issue 2, December 2009, Page(s):37 - 38 Digital Object Identifier 10.1109/L-CA.2009.60

[N29] C. Cérin, K.C. Li, and J-L. Gaudiot, "Secure, Manageable and Controllable Grid Services," *Journal of Supercomputing / Special Issue on Secure, manageable and controllable grid services*, DOI: 10.1007/s11227-009-0311-8, July 2009.

[N28] J-L. Gaudiot, "The Walls of Computer Design, (abstract)," *Lecture Notes in Computer Science,* Volume 4330/2006, pp.1, *Proceedings of 2006 International Symposium on Parallel and Distributed Processing and Applications (ISPA 2006),* Sorrento, Italy, December 4-7, 2006.

[N27] M. Hill, J-L. Gaudiot, M. Hall, J. Marks, P. Prinetto, and D. Baglio, "A Wiki for Discussing and Promoting Best Practices in Research," in *Communications of the ACM,* Volume 49, Issue 9, pp. 63-64, September 2006.

[N26] J-L. Gaudiot, "Introduction, Special Issue Nineteenth International Parallel and Distributed Processing Symposium - IPDPS 2005," in *Journal of Parallel and Distributed Computing,* Volume 66, Issue 7, Page 873, July 2006.

[N25] J-L. Gaudiot, Y. Patt, and K. Skadron, "Foreword," *IEEE Computer Architecture Letters*, Vol. 5, No. 1, pp. 1, January-June 2006.

[N24] J-L. Gaudiot, "Commentary for the paper -Software Simulation of DNA-Based Killer Automaton: The Innovative Nanomedicine- by Shaoshan Liu," *The UCI Undergraduate Research Journal*, Volume VIII, 2005.

[N23] J-L. Gaudiot and S-W. Song, "Message from the Guest Editors," *International Journal on Parallel Programming - Special Issue on Computer Architecture*, October 2005.

[N22] J-L. Gaudiot, "Message from the Program Chair," *International Parallel and Distributed Processing Symposium*, Denver, Colorado, April 2005.

[N21] J-L. Gaudiot and K.C. Li, "Foreword from the Guest Editors," *International Journal of Computer Applications in Technology - Special Issue on Applications for High-Performance Systems*, Second Semester, 2004.

[N20] J-L. Gaudiot and S.W. Song, "Message from the Program Chairs," *Symposium on Computer Architecture and High Performance Computing (SBAC-PAD 2004)*, Foz do Iguaçu, Brazil, October 2004.

[N19] J-L. Gaudiot, "Preface," *Note from the Program and General Chairs of the Conference on Computing Frontiers (CF '04)*, Ischia, Italy, April 2004.

[N18] J-L. Gaudiot, "Introducing the New Editor-in-Chief of the IEEE Transactions on Computers," *IEEE Transactions on Computers*, Vol. 52, No. 1, pp. 1-2, January 2003.

[N17] J-L. Gaudiot, "Parallel Computer Architecture and Instruction-Level Parallelism (Topic Program Chair's message)," *Proceedings of the Eight International Euro-Par Conference (Euro-Par '02)*, pp. 457, Paderborn, Germany, August 2002.

[N16] J-L. Gaudiot, "Editor's Note," *IEEE Transactions on Computers*, Vol. 51, No. 11, pp. 1281, November 2002.

[N15] J-L. Gaudiot, "Editor's Note," *IEEE Transactions on Computers*, Vol. 51, No. 7, pp. 737-739, July 2002.

[N14] J-L. Gaudiot, "Editor's Note," *IEEE Transactions on Computers*, Vol. 51, No. 1, pp. 1-2, January 2002.

[N13] J-L. Gaudiot "Editor's Note," *IEEE Transactions on Computers*, Vol. 50, No. 9, pp. 863-864, September 2001.

[N12] J-L. Gaudiot "Editor's Note," *IEEE Transactions on Computers*, Vol. 50, No. 4, pp. 289-291, April 2001.

[N11] M. Cosnard, U. Finger, and J-L. Gaudiot, "IFIP Special Issue: Editorial Note," *Parallel Processing Letters*, Vol. 11, No. 1, pp. 3-5, March 2001.

[N10] J-L. Gaudiot "Editor's Note," *IEEE Transactions on Computers*, Vol. 49, No. 10, pp. 1009-1012, October 2000.

[N9] J-L. Gaudiot "Editor's Note," *IEEE Transactions on Computers*, Vol. 49, No. 5, pp. 385-386, May 2000.

[N8] J-L. Gaudiot "Editor's Note," *IEEE Transactions on Computers*, Vol. 49, No. 2, pp. 97-99, February 2000.

[N7] J-L. Gaudiot and F. Lombardi, "Guest Editors' introduction," *IEEE Transactions on Computers*, Vol. 48, No. 6, pp. 553-555, June 1999.

[N6] J-L. Gaudiot, "Special topics on Parallel Architectures and Compilation Techniques (Guest editor's introduction)," *International Journal of Parallel Programming*, Vol. 24, No. 3, pp. 207-208, June 1996.

[N5] J-L. Gaudiot, L. Bic, and P. Evripidou, "Preface," in *Proceedings of the 1995 Conference on Paralel Architectures and Compilation Techniques*, Limassol, Cyprus, June 1995.

[N4] G.R. Gao, J-L. Gaudiot, and L. Bic, "Special Issue on Data-Flow and Multithreaded Systems (Guest editors' introduction)," *Journal of Parallel and Distributed Computing*, Vol. 18, No. 3, pp. 271-272, December 1993.

[N3] S. Bhatt, J-L. Gaudiot, L. Patnaik, and M. Reeve, "Program Chairs' message," in *Proceedings of the Fifth IEEE Symposium on Parallel and Distributed Processing*, Dallas, Texas, December 1993.

[N2] K. Ebcioğlu and J-L. Gaudiot, "Preface," in *Proceedings of the IFIP WG10.3 Working Conference on Architectures and Compilation Techniques for Fine and Medium Grain Parallelism*, Orlando, Florida, January 1993.

[N1] L. Bic and J-L. Gaudiot, "Special topics on data-flow systems (Guest editors' introduction)," *Journal of Parallel and Distributed Computing*, Vol. 10, No. 4, pp. 277-278, December 1990.

Invited Presentations

- "Creating Autonomous Vehicle Systems," Invited speaker at the 2018 National Conference Embedded Systems, HUST, Wuhan, PRC, September 14, 2018.

- "Creating Autonomous Vehicle Systems," Invited speaker at Universidade de São Paulo, São Paulo, Brazil, June 27, 2018.

- "Creating Autonomous Vehicle Systems," Invited speaker at IEEE Symposium on Computers and Communications, Natal, Brazil, June 27, 2018.

- "Year in Review," Computer Society Learning Series Webinar, Tuesday, 5 December at 12:00 PM ET.

- "Future Research Directions in Computing," Invited speaker at the National Science Foundation, Washington, DC, November 28, 2017.

- "Creating Autonomous Vehicle Systems," Invited speaker at CNCC, Fuzhou, PRC, October 26, 2017.

- "SPARTA: a Stream-based Processor And Run-Time Architecture," Keynote Speaker at SBAC-PAD, Campinas, Brazil, October 18, 2017.

- "SPARTA: a Stream-based Processor And Run-Time Architecture," Invited Speaker at the University of Brasilia, Brazil, October 17, 2017.

- "SPARTA: a Stream-based Processor And Run-Time Architecture," Keynote Speaker at the Seminar, Informatique, Paralllisme et Architectures, Marne-la-Vallée, September 21, 2017.

- "Creating Autonomous Vehicle Systems," Invited speaker at ESIEE, Marne-la-Vallée, September 12, 2017.

- "Computing Education: IEEE HKN and IEEE CS," Presentation to the IEEE-HKN Special Panel: Computing Education: the IEEE-HKN Perspective at the 2017 IEEE 41st Annual Computer Software & Applications Conference (COMPSAC 2017), Torino, Italy, July 6, 2017.

- "SPARTA: a Stream-based Processor And Run-Time Architecture," Keynote Speaker at the 7th International Scientific Conference, Education, Science, Innovations (ESI 2017), Pernik, Bulgaria, June 9-10, 2017.

- "Hardware and Software Issues in the Future," Distinguished Speaker for a series of lectures at the University of Bologna, Bologna, Italy, April 27-28, 2017.

- "SPARTA: a Stream-based Processor And Run-Time Architecture," Keynote Speaker at the 14th International Conference on Information Technology : New Generations (ITNG 2017), Las Vegas, Nevada, USA, April 10-12, 2017.

- "SPARTA: a Stream-based Processor And Run-Time Architecture," Keynote Speaker at the 79th National Convention of the Information Processing Society of Japan (IPSJ) Congress, Nagoya, Japan, March 16, 2017.

- "SPARTA: a Stream-based Processor And Run-Time Architecture," Invited Presentation at Waseda University, Tokyo, Japan, March 15, 2017.

- "SPARTA: a Stream-based Processor And Run-Time Architecture," Invited Presentation at Hitachi Central Research Labs, Tokyo, Japan, March 14, 2017.

- Keynote speaker at INDICON 2017, Bangalore, India, December 18, 2016.

- Keynote Speaker at All India Computer Society Congress (AICSC 2016), Hyderabad, India, December 15, 2016.

- Keynote speaker at the 2016 IEEE Conference on Teaching, Assessment, and Learning for Engineering (TALE 2016), Bangkok, Thailand, December 2016.

- "Technology Considerations for Energy-Efficiency and Performance in Computer Architecture," Distinguished Lecturer at University of Westminster, UK, December 2016.

- "Lectures in Computer Architecture," Distinguished Speaker at University of Bologna, Italy, October 26, 2016.

- Invited at the NSF sponsored Workshop on Architecture and Software for Emerging Applications (WASEA), in conjunction with the Twenty Fifth Parallel Architecture and Compiler Techniques (PACT) conference, Haifa, Israel, September 2016.

- "Technology Considerations in Computer Architecture," Distinguished Speaker at University of Macau, Macau, September 2016.

- "Architectural Trends for Digital Systems in the new Era," Distinguished Speaker at Dong Hwa University, Taiwan, September 2016.

- "Architectural Trends for Digital Systems in the new Era," Distinguished Speaker at National Taiwan University, Taiwan, September 2016.

- "Architectural Trends for Digital Systems in the new Era," Distinguished Speaker at National Tsing-Hua University, Taiwan, September 2016.

- "Architectural Trends for Digital Systems in the new Era," Distinguished Speaker at Academia Sinica, Taipei, Taiwan, September 2016.

- "New Design Techniques in the post-Moore's Law Era," Keynote Speaker at the *Fourth IEEE International Symposium on Parallel and Distributed Processing with Applications* (IEEE ISPA-16), Tianjin, China, August 23-26, 2016.

- "New Design Techniques in the post-Moore's Law Era," Distinguished Speaker at Nagoya Institute of Technology, Nagoya, Japan, August 21, 2016.

- Member of the panel "Rebooting Computing," at COMPSAC 2016, Atlanta, GA, June 11, 2016.

- "Technology Considerations in Computer Architecture," Invited Speaker at Georgia Institute of Technology, June 6, 2016.

- "SPARTA: A Dataflow-Inspired System Design," Distinguished CS and ECE Seminar Speaker, Illinois Institute of Technology, Chicago, IL, May 6, 2016.

- "SPARTA: A Dataflow-Inspired System Design," Invited Speaker at Colorado State University, Fort Collins, CO, May 3, 2016.

- "Technology Considerations in Computer Architecture," ISTeC Distinguished Lecturer, Colorado State University, Fort Collins, CO, May 2, 2016.

- "Technology Considerations in Computer Architecture," Invited Speaker at the University of Chicago, Chicago, IL, April 18, 2016.

- "Trends in Electronics," Distinguished Speaker for a series of lectures at the University of Bologna, Bologna, Italy, March 21-22, 2016.

- "Technology Considerations in Computer Architecture," Invited Speaker at Technion - Israel Institute of Technology, Haifa, Israel, March 16, 2016.

- "Technology Considerations in Computer Architecture," Distinguished Speaker at Texas A&M University, College Station, TX, March 9, 2016.

- "Technology Considerations in Computer Architecture," Distinguished Lecture at the George Washington University, Washington, DC, February 18, 2016.

- "Technology Considerations in Computer Architecture," Invited talk at the University of Paris V, Paris, France, January 17, 2016.

- "Technology Considerations in Computer Architecture," Invited talk at the University of Augsburg, Augsburg, Germany, January 14, 2016.

- "Technology Considerations in Computer Architecture," Invited talk at the University of Chicago Loyola, Chicago, IL, November 24, 2015.

- "Energy Efficiency in Embedded System Design," Keynote talk at BDCloud 2015 & FCST 2015, Dalian, PRC, August 2015.

- Member of the panel "Rebooting Computing," at COMPSAC 2015, Taichung, Taiwan, July 2015.

- "Energy Efficiency in Embedded System Design," Invited talk at National Cheng Kung University, Tainan, Taiwan, July 2015.

- "Energy Efficiency in Embedded System Design," Invited talk at the University of Bologna, Italy, March 25-27, 2015.

- Keynote Speaker at the Sixth International Supercomputing Conference in Mexico (ISUM 2015), Mexico City, Mexico, March 9-12, 2015.

- "Energy Efficiency in Embedded System Design," Invited talk at Technical University of Crete, Chania, Greece, July 7, 2014.

- "Energy Efficiency in Embedded System Design," Invited talk at IBM T.J. Watson Research Center, Ossining, NY, May 20, 2014.

- "EHA: The Extremely Heterogeneous Architecture," Invited talk at the Svoboda series of distinguished lectures, Czech Technical University in Prague, Prague, Czech Republic, November 12-14, 2013.

- "EHA: The Extremely Heterogeneous Architecture," Invited for a series of presentations at the University of Bologna, Italy, March 25-27, 2013.

- "EHA: The Extremely Heterogeneous Architecture," Keynote presentation at the 2012 International Symposium on Pervasive Systems, Algorithms, and Networks (ISPAN 2012), San Marcos, Texas, December 13-15, 2012.

- "Scheduling Optimization in Multicore Multithreaded Microprocessors through Dynamic Modeling," Invited presentation at the Symposium Multicore Architectures and Their Effective Operation 2012, Barcelona, Spain, June 28-29, 2012.

- "Fighting Amdahl's law in many-core and GPU parallel architectures with value prediction," Keynote Presentation at the Ninth IEEEACS International Conference on Computer Systems and Applications (AICCSA), DOI: 10.1109AICCSA.2011.6126642, Sharm-el-Sheik, Egypt, December 2011.

- "Value Prediction in Parallel Architectures," Keynote Presentation at the Eight IFIP International Conference on Network and Parallel Computing (NPC 2011), Changsha, PR China, October 21-23, 2011.

- "Value Prediction in Parallel Architectures," Keynote Presentation at the Fourteenth IEEE International Conference on Computational Science and Engineering (CSE-2011), Dalian, PR China, August 24, 2011.

- "Languages, Compilation, and Models of Computation for Exascale Systems," Invited Presentation at the 2011 DOE Workshop on Architectures II on Exascale and Beyond: Configuring, Reasoning, Scaling, Sandia National Laboratory, Albuquerque, NM, August 8-10, 2011.

- Invited for a series of presentations at Kuwait University, Kuwait, April 5-13, 2011.

- "Value Prediction in Parallel Architectures," Keynote Presentation at AMINA 2010, Monastir, Tunisia, November 19, 2010.

- "Value Prediction in Parallel Architectures," Invited Presentation at Huazhong University of Science & Technology (HUST), Wuhan, PR China, September 2010.

- "Value Prediction in Parallel Architectures," Invited Presentation at Tsinghua University, Beijing, PR China, September 2010.

- "Value Prediction in Parallel Architectures," Invited Presentation at EURECOM, Sophia-Antipolis, France, June 2010.

- "Strategic Planning in the Department of Electrical Engineering and Computer Science at the University of California, Irvine," IEMN, Lille, France, May 2010.

- "Value Prediction in Parallel Architectures," Invited Presentation at the University of Barcelona, Barcelona, Spain, April 2010.

- "Value Prediction in Parallel Architectures," Invited Presentation at INRIA, Saclay, France, April 2010.

- "Value Prediction in Parallel Architectures," Invited Presentation at ESIEE, Marne-la-Vallée, France, April 2010.

- "Value Prediction in Parallel Architectures," Invited Talk at Toulouse '09, Toulouse, France, September 2009.

- "The Walls of Computer Design," Keynote Talk at the Fourth Workshop on Grid Technologies and Applications (WoGTA?07), Providence University, Taichung, Taiwan, December 2007.

- "The Walls of Computer Design," Invited Presentation at Tsinghua National University, Taipei, Taiwan, December 2007.

- "The Walls of Computer Design," Invited Presentation at Tatung University, Taipei, Taiwan, December 2007.

- "The Walls of Computer Design," Invited Presentation at Seoul National University, Seoul, Korea, August 22, 2007.

- "The Walls of Computer Design," Keynote Speech at the Fourth International Symposium on Parallel and Distributed Processing and Applications (ISPA 2006), Sorrento, Italy, December 2006.

- "The Walls of Computer Design," Invited tutorial lecture at the International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD 2006), Ouro Preto, Brazil, October 2006.

- "Design and Effectiveness of Small-Sized Decoupled Dispatch Queues," Joint Presentation to the Electrical and Computer Engineering Department and the Computer Science Department at Colorado State University, Fort Collins, Colorado, October 10, 2006.

- "The Walls of Computer Design," Information Science and Technology Center (ISTeC) Distinguished Lecture, Colorado State University, Fort Collins, Colorado, October 9, 2006.

- "The Walls of Computer Design," Invited tutorial lecture at the IEEE 2006 John Vincent Atanasoff International Symposium on Modern Computing, Sofia, Bulgaria, October 3, 2006.

- "The Walls of Computer Design," Invited presentation at the *École Nationale Supérieure de Techniques Avancées* (ENSTA), Paris, France, January 3, 2006.

- "SPEAR: A Hybrid Model for Speculative Pre-Execution," Invited presentation at the IFIP WG10.3 Meeting, Paris, France, February 2005.

- "Novel Architectures," 2002 Southern California Embedded Systems Seminar, September 2002.

- "I-Structure Software Caches," 2002 Parallel Processing and Computer Architecture Workshop, Irvine, California, March 2002.

- "Power Aware SMT Architectures," Invited talk at the Computer Science Department, University of California, Riverside, February 2002.

- "The Memory Gap: To tolerate or to Reduce?," Invited presentation at Raytheon, Inc., El Segundo, California, April 2002.

- "I-Structure Software Caches," Invited presentation at CICESE, Ensenada, Mexico, April 2002.

- "Power Aware Design," Invited presentation at the International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD 2001), Pirenópolis, September 2001.

- "The Memory Gap: To Tolerate or to Reduce?," University of California, Irvine, May 2001.

- "Memory Latency: To Tolerate or to Reduce?," Distinguished lecture at Rochester Institute of Technology, Rochester, NY, February 5th, 2001.

- "Memory Latency: To Tolerate or to Reduce?," Keynote presentation at the International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD 2000), São Pedro, Brazil, October 2000.

- "Parallelism and Multithreaded architectures," Invited presentation at the Universidade de São Paulo, Brazil, October 1999.

- "Parallelism and Multithreaded architectures," Invited presentation at the Universidade Federal de Pernambuco, Recife, Brazil, October 1999.

- "Parallelism and Multithreaded architectures," Keynote presentation at the Simpósio Brasileiro de Arquitetura de Computadores e Processamento de Alto Desempenho (SBAC-PAD), Natal, Brazil, October 1999.

- 'Parallelism and Multithreaded Architectures," Presented at the SIAM CSE 2000, Washington, DC, September 1999.

- "Does SMT pull its weight? a bottom-up analysis," Invited presentation at Vrije Univ. Brussels, Brussels, Belgium, May 1999.

- "Future Computer Architectures," Keynote presentation at the 1998 international conference on computers, communications and systems, Taegu, Korea, November 1998.

- "I-Structure Software Caches," Invited presentation at Kyungpook National University, Korea, November 1998.

- "ISSC Implementation on EARTH," University of Delaware, November 1998.

- "I-Structure Software Caches," University of Adelaide, Australia, July 1998.

- "I-Structure Software Caches," Université Paris VII, Paris, France, May 1998.

- "Simultaneous Multithreading for Digital Signal Processing," Rockwell Semiconductor Systems, Newport Beach, California, March 1998.

- "I-Structure Software Caches," IMAG, Grenoble, France, December 1997.

- "I-Structure Software Caches," LAAS, Toulouse, France, December 1997.

- "I-Structure Software Caches," Université de Picardie, Amiens, France, November 1997.

- "The Sisal Model of Functional Programming and its Implementation," IRISA, Rennes, France, October 1997.

- "Compilation for SMT Architectures," University of Cyprus, Larnaca, Cyprus, July 1997.

- "Compilation for SMT Architectures," INRIA, Rocquencourt, France, June 1997.

- "I-Structure Software Caches," Université PARIS VII, Paris, France, May 1997.

- "I-Structure Software Caches," INRIA Sophia-Antipolis, Sophia Antipolis, France, May 1997.

- "I-Structure Software Caches," University of Texas, Arlington, April 1997.

- "Parallel Computing: One Opportunity, Four Challenges," Yonsei University, Seoul, Korea, March 1997.

- "Parallel Computing: One Opportunity, Four Challenges," Seoul National University, Seoul, Korea, March 1997.

- "Parallel Computing: One Opportunity, Four Challenges," ETRI, Korea, March 1997.

- "Multithreaded Execution for Multiprocessors and Superscalar Architectures," ETRI, Korea, March 1997.

- "Making Parallel Functional Computing a Reality: the SISAL Project," Invited presentation at the Second Parallel Architectures/Algorithms Symposium, Aizu-Wakamatsu, Japan, March 1997.

- "I-Structure Software Cache and Nomadic Threads," SOCAL Parallel Processing Workshop, December 1996.

- "Making Functional Programming a Reality: The Sisal Project," Distinguished Visitor Presentation at Purdue University, November 1996.

- "I-Structure Software Caches," Distinguished Visitor Presentation at Purdue University, November 1996.

- "Parallel Computing: One Opportunity, Four Challenges," University of Massachusetts, Lowell, Massachusetts, October 1996.

- "I-Structure Software Caches," MITRE Corporation, Massachusetts, October 1996.

- "Data-Driven Logic Programming," Bridgewater State College, January 1995.

- "Parallel Computing: One Opportunity, Four Challenges," Distinguished Visitor Presentation at the IEEE Northeastern Michigan section, Wayne State University, November 1995.

- "Making Parallel Functional Computing a Reality: the SISAL Project," Invited presentation at the University of Illinois, CSRD, November 1995.

- "Parallel Computing: One Opportunity, Four Challenges," Distinguished Visitor Presentation at the IEEE Orlando section, University of Central Florida, September 1995.

- "Data-flow and Multithreaded Multiprocessors," Distinguished Visitor Presentation at the IEEE Dallas section, University of Texas at Arlington, March 1995.

- "Data-Driven Programming of Distributed Memory Multiprocessors," Distinguished Visitor Presentation at the IEEE Northeastern Michigan section, Oakland State University, March 1995.

- "Parallel Computing: One Opportunity, Four Challenges," Distinguished Visitor Presentation at the IEEE Boston section, January 1995.

- "Structure Handling in Multithreaded Architectures," Distinguished Visitor presentation at *State University of New York*, Buffalo, New York, December 1994.

- "Parallel Computing: One opportunity, Four (no! six) Challenges," *INRIA*, Sophia Antipolis, France, June 1994.

- "Issues in Parallel Computing," Distinguished lecture at *Southern Methodist University,* December 1993.

- "Data-Driven and Multithreaded Architectures for High-Performance Computing," Invited presentation at *The International Summer School on Parallel Systems and Languages (ISS PLANS),* Prague, Czech Republic, July 1993.

- "Parallel Computing and Programmability Issues," *Kubota Pacific Computers,* May 7, 1992.

- "Highly Programmable Architectures for Knowledge-Based and Natural Language Processing," *Workshop on Intelligent Information Systems,* Rome, New York, Oct. 1991.

- "Data-Driven Programming of Distributed Memory Multiprocessors," Invited presentation at the *NATO Advanced Summer Institute,* Ankara, Turkey, July 1991.

- "Message-Passing Multiprocessors," *Journées d'études Architecture Parallelisme et Images,* Paris, France, December 1990.

- "Mapping directed graphs based computations onto a reduced VLSI architecture," Poster presentation at the *International Workshop on Algorithms and Parallel VLSI Architectures*, Pont-à-Mousson, France, June 1990.

- "Data Structure Handling in Data-Flow Systems," *INRIA*, Rocquencourt, France, December 1989.

Ph.D. students graduated

- Howard Wong, Fall 2017
  Dissertation title: *Characterizing Memory Usage Behavior in Memory-related Code Changes*

- Shouq Alsubaihi, Spring 2017
  Dissertation title:*Performance, Energy and Temperature Considerations for Job Scheduling and for Workload Distribution in Heterogeneous Systems*

- Ganghee Jang, Spring 2016
  Dissertation title: *Scalability Issues in the Design of Many-Core Processors*

- Myeoung Seo Kim, Spring 2016
  Dissertation title: *I/O Design and Core Power Management Issues in Heterogeneous Multi/Many-Core System-on-Chip*

- Jed Kao-Tung Chang, Winter 2012
  Dissertation title: *Flexible Architectures for Enhanced Security*

- Shaoshan Liu, Winter 2010
  Dissertation title: *Value Prediction in Many Core Systems*

- Chen Liu, Summer 2007
  Dissertation title: *Dynamic Partitioning in Simultaneous MultiThreaded Architectures*

- Kyueun Yi, Winter 2007
  Dissertation title: *Network Applications on Modern Computer Architectures*

- Xiaobin Li, Summer 2005
  Dissertation title: *Tolerating Radiation-Induced Transient Faults in Modern Processors*

- Dongsoo Kang, Spring 2004
  Dissertation title: *Speculation-Aware Thread Scheduling for SMT*

- Ihn Kim, Fall 2003
  Dissertation title: *VMINI: Virtual Memory Integrated Network Interface*

- Won Woo Ro, Fall 2003
  Dissertation title: *Decoupled Memory Access Architectures with Speculative Pre-Execution*

- Jung-Yup Kang, Fall 2003
  Dissertation title: *Efficient PIM (Processor-In-Memory) Architectures for Data-Intensive Applications*

- SeongWon Lee, Spring 2003
  Dissertation title: *Solving Power Problems in High Performance Multithreaded Architectures*

- Chulho Shin, Fall 2002
  Dissertation title: *Adaptive Dynamic Thread Scheduling for Simultaneous Multithreaded Architectures with a Detector Thread*

- JongWook Woo, Spring 2001
  Dissertation title: *Alias Analysis for Java with Reference-Set Representation in High Performance Computing*

- Steve Jenks, Fall 2000
  Dissertation title: *Compiler Controlled Locality Exploitation using Thread Migration for Distributed Memory Parallel Computers*

- James Burns, Fall 1999
  Dissertation title: *POSM: Parallel On-chip Simultaneous Multithreading*

- Wen-Yen Lin, Fall 1999
  Dissertation title: *I-Structure Software Caches: Exploiting Global Data Locality in Non-Blocking Multithreaded Architectures*

- Chung-Ta Cheng, Fall 1999
  Dissertation title: *Architectural Support for Network-based Computing*

- Halima ElNaga, Fall 1998
  Dissertation title: *MCOMA: A Multithreaded Cache Only Memory Architecture*

- Hung-Yu Tseng, Spring 1998
  Dissertation title: *Automatic Array Partitioning and Distributed-array Compilation for Efficient Communication*

- Hiechel Kim, Summer 1996
  Dissertation title: *High Performance Parallel Logic Programming on Distributed Shared Memory Multiprocessors*

- Moez Ayed, Summer 1996
  Dissertation title: *Automatic Code Partitioning for Distributed Memory Multiprocessors*

- Namhoon Yoo, Summer 1996
  Dissertation title: *Parallelism Control in Multithreaded Multiprocessors*

- Dae-Kyun Yoon, Spring 1996
  Dissertation title: *A Framework for Coarse-Grain Parallel Execution of Functional Programs*

- Yung-Syau Chen, Spring 1996
  Dissertation title: *Stateful Computations in Functional Languages*

- ChinHyun Kim, Spring 1994
  Dissertation title: *Functional Programming and Fine-Grain Multithreading for High Performance Parallel Computing*

- Walter Tackett, Spring 1994
  Dissertation title: *Recombination, Selection, and the Genetic Construction of Computer Programs*

- Soheil Shams, Summer 1992
  Dissertation title: *Dream Machine - A Platform for Efficient Implementation of Neural Networks with Arbitrary Complex Interconnection Networks*

- Ken Flaton, Summer 1992
  Dissertation title: *2D Object Recognition by Adaptive Feature Extraction and Dynamical Link Graph Matching*

- Andrew Sohn, Summer 1991
  Dissertation title: *Parallel Processing of Production Systems on Data-Flow Multiprocessors*

- Chih-Ming Lin, Spring 1991
  Dissertation title: *Numerical Partial Differential Equations Solvers on Variable-Grain Data-Flow Multiprocessor systems*

- Paraskevas Evripidou, Fall 1990
  Dissertation title: *On Scheduling, Granularity, and State-Operations of Hybrid Data-Flow / Control-Flow Systems*

- Liang-Teh Lee, Summer 1989
  Dissertation title: *Occamflow: Programming a Multiprocessor System in a High-Level Data-Flow Language*

- Walid Najjar, Summer 1988
  Dissertation title: *Fault-Tolerance and Reliability Analysis of Large-Scale Multicomputer Systems*

- Yi-Hsiu Wei, Spring 1988
  Dissertation title: *Demand-Driven Evaluation of Functional Programs in Data-Flow Multiprocessors*

Teaching activities

- USC Classes (until December 2001):

  - EE599/653 Functional programming and data-flow systems (graduate level)
  - EE557 Computer architecture (graduate level)
  - EE454 Introduction to system design using microprocessors (undergraduate level)
  - EE457 Computer architecture (undergraduate level)
  - EE557b Advanced computer architecture (graduate level)

- UCI Classes (since January 2002):

  - ECE 259 Microarchitecture and Compilation Techniques for Parallel Processing
  - EECS 31 (formerly ECE 31) Introduction to Digital Systems Design
  - EECS 117 (formerly ECE137) Parallel Computer Systems
  - EECS 213 Computer Architecture
  - EECS 31L Digital Systems Design Lab
  - EECS 221 Advanced Computer Architecture

- Introduced a new class (Functional Programming and Data-Flow Systems) (graduate level)

- Developing a multimedia Web site for EECS 31 (Introduction to Digital Systems Design)

Short-term Instruction

- "The Walls of Computer Design," Short course at Tunghai University, Taichung, Taiwan, July 2005

- "Data-driven and multithreaded architectures for high-performance computing," Invited tutorial at the *IV Brazilian Symposium in Computer Architectures, High Performance Computing,* São Paulo, Brazil, October 1992

- "Data-driven and multithreaded architectures for high-performance computing," Invited tutorial at the *VAPP/CONPAR '92 Joint Conference on Vector and Parallel Processing,* Lyons, France, September 1992

- USC ITV satellite course on *Parallel Computing,* February 5, 1991

- Tutorial on data-flow systems associated with the *1989 ACM International Symposium on Computer Architecture,* Jerusalem, Israel, June 1989

- USC ITV satellite course on *Implementation of Artificial Neural Networks,* April 13, 1989 (with C. von der Malsburg)

- USC ITV satellite course on *Parallel Computing,* March 9, 1989

- USC Extension (1984 and 1987): Short course on parallel processing (1 day session)

Conference Organization and General Chairmanship

- Co-general chairman of the Twenty Eighth International Symposium on Computer Architecture and High Performance Computing, Marina Del Rey, CA, October 26-28, 2016

- Co-general chairman of the Fourteenth IEEE International Symposium on Parallel and Distributed Processing with Applications (IEEE ISPA-16), Tianjin, PRC, August 23-26, 2016

- Co-general chairman of the 2016 International Workshop on Hardware/Software Interface for Internet of Things and Big Data, Philadelphia, PA, August 16-19, 2016

- Co-general chairman of the Fifth IEEE International Conference Big Data and Cloud Computing (BDCloud 2015), Dalian, PRC, August 26-29, 2015

- Co-general chairman of the Fourteenth IEEE International Conference on Computational Science and Engineering (CSE-2011), Dalian, PRC, August 24-26, 2011

- Co-general chairman of the Seventh IFIP International Conference on Network and Parallel Computing (NPC 2010), Zhengzhou, PRC, September 13-15, 2010

- Co-general chairman of the Fourth IFIP International Conference on Network and Parallel Computing (NPC 2007), Dalian, PRC, September 18-21, 2007

- Co-general chairman of the Second IFIP International Conference on Network and Parallel Computing (NPC 2005), Beijing, PRC, November 30 - December 2, 2005

- Co-chair of WEPA-1: First Workshop on Embedded Parallel Architectures, held in conjunction with the Tenth International Symposium on High Performance Computer Architecture, Madrid, Spain, February 14, 2004

- Co-organizer with Dr. Stephen Jenks of the Southern California Parallel Processing and Computer Architecture Workshop, March 2002

- Chairman of the 1990 IFIP Working Group 10.3 Workshop, Paris, France, February 2000

- Co-chairman of the December 1996 SoCal Parallel Processing Workshop, held at the University of Southern California, December 1996

- Chairman of the 1996 IFIP Working Group 10.3 workshop, Paris, France, February 1996

- Co-chairman of the Workshop on Data-Flow Systems and Multithreading associated with the *1996 High Performance Computer Architecture Symposium,* San Jose, California, February 1996

- Co-chairman of the Workshop on Data-Flow Systems and Multithreading associated with the *1992 International Symposium on Computer Architecture,* Gold Coast, Australia, May 1992

- Co-general chairman of the *1992 International Symposium on Computer Architecture*, Gold Coast, Australia, May 1992

- Co-chairman of the Workshop "Data-flow computing: a status report," associated with the *1989 ACM International Symposium on Computer Architecture,* Jerusalem, Israel, June 1989

Program Committee Chairmanships

- Co-Organizer of a Special Session "Creating Autonomous Vehicle Systems," at COMP-SAC 2018, Tokyo, Japan, July 2018

- Co-Program Chair of the 2013 International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD 2013), Porto de Galinhas, Pernambuco, Brazil, October 2013

- Co-Program Chair of the 2011 International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD 2011), Vitória, Espirito Santo, Brazil, October 2011

- Co-Program Chair of the 2007 International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD 2007), Gramado, Brazil, October 2007

- Program Chair of the Nineteenth International Symposium on Parallel and Distributed Processing Systems (IPDPS 2005), Denver, Colorado, April 2005

- Co-Program Chair of the 2004 International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD), Foz do Iguaçu, Brazil, October 2004

- Co-Program Chair of the 2004 Computing Frontiers Conference (CF '04), Ischia, Italy, June 2004

- Co-Program Chair of the First Workshop on Embedded Parallel Architectures (WEPA-1) held in conjunction with the Tenth International Symposium on High Performance Computer Architecture, Madrid, Spain, February 14, 2004

- Topic Program Chair of the "Topic 8: Parallel Computer Architecture and Instruction-Level Parallelism," held at the Eighth International Euro-Par Conference (Euro-Par '02), Paderborn, Germany, August 27-30, 2002

- Program Committee Chair of the 1999 High Performance Computer Architecture conference (HPCA), Orlando, Florida, January 1999

- Chairman of the Program Committee for the 1995 Conference on Parallel Architectures and Compilation Techniques (PACT), Limassol, Cyprus, June 1995

- Chairman of the Program Committee (Systems Track) for the 1993 IEEE International Symposium on Parallel and Distributed Computing, Arlington, Texas, December 1993

- Chairman of the Program Committee for the 1993 IFIP Working Conference on Architectures and Compilation Techniques for Fine and Medium Grain Parallelism, Orlando, Florida, January 1993

Editorships

- Co-Guest Editor of a special issue (Reconfigurability and Power Issues in Computer Systems Design), *Computing Now,* November 2014

- Advisory Board member of the IJES International Journal of Embedded Systems

- Co-Guest Editor of a Special Issue of the Journal of Parallel Programming on the Twenty First International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD 2011), 2012

- Regional Editor (North America), International Journal of Computational Science and Engineering

- Co-Guest Editor of a Special Issue of the Journal of Parallel Programming on the Nineteenth International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD 2007), 2009

- Co-Guest Editor of a Special Issue of the Journal of Supercomputing on Secure, Manageable and Controllable Grid Services, 2009

- Co-Guest Editor of a Special Issue of the Journal of Supercomputing (NPC 2007), 2007

- Co-Guest Editor of a Special Issue of the Journal of Parallel and Distributed Processing, 2005

- Co-Guest Editor (with Siang Wun Song) of a Special Issue of the International Journal of Parallel and Distributed Programming, 2005

- Co-founder and founding Editor-in-Chief of *IEEE Computer Architecture Letters*, 2006-2009

- Co-Guest editor of a Special Issue of the International Journal of Computer Applications in Technology, *Applications for High Performance Systems,* Fourth Quarter 2004

- Editor-in-Chief of the IEEE Transactions on Computers (1999 - 2002)

- Editorial Board Scientific Programming (Wiley)

- Editorial Board Parallel Processing Letters

- Editorial Board International Journal on Artificial Intelligence Tools

- Co-Guest Editor of a Special Issue on Parallel Processing in the New Millennium, Parallel Processing Letters, Vol. 11, Number 1, March 2001.

- Co-Guest Editor of a Special Issue of the Parallel Processing Letters, *IFIP WG10.3 Workshop,* March 2001

- Co-Guest Editor of a Special Issue of the IEEE Transactions on Computers, *Reconfigurable Computing,* June 1999.

- Co-Guest Editor of a Special Issue of the IEEE Transactions on Computers, *Multithreaded Computing,* June 1999.

- Guest Editor of a Special Issue of the International Journal of Parallel Programming, *Parallel Architectures and Compilation Techniques,* June 1996

- Associate Editor of the IEEE Transactions on Computers (1994-1998)

Other Professional Activities

- Committee member of the International Peer Review of the Computer Science Discipline, Tianjin University, Tianjin, PRC, May 15-16, 2018

- 2018 TAB Representative and Member of the IEEE Publication Services and Products Board (PSPB)

- IEEE Computer Society President (2017)

- Member of the Fifth Prague Embedded Systems Workshop (PESW) Program Committee

- Chair of COMPSAC EIC Committee, January 2015 - December 2016

- Member of COMPSAC Plenary Panel - Rebooting Computing, COMPSAC 2016, June 2016

- Member of the 2016 IEEE Computer Society Research Advisory Board

- IEEE Computer Society President-Elect (2016)

- Invited speaker at Professor Louri's installation as Kalgaard Professor at George Washington University, September 9, 2015

- Member of the Prix d'excellence du CA de l'TS, September 2015

- Member of COMPSAC Plenary Panel - Rebooting Computing, COMPSAC 2015, July 2015

- IEEE Computer Society Representative to the USA Committee on Research & Development Policy Committee (2015 - 2016)

- Representative to the Council on RFID, IEEE Computer Society (2015)

- Member of the steering committee for the International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD)

- Member of the IEEE TAB/PSPB Products and Services Committee - IEEE Computer Society Representative (2015)

- Member of the Program Committee of the Twenty-Sixth International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD), Paris, France, October 2014

- Member of a review panel for the National Science Foundation, 2014

- Member of the Program Committee of the Second Prague Embedded Systems Workshop (PESW 2014), Roztoky u Prahy, Czech Republic, June 12-14, 2014

- Vice-President and Chair, IEEE Computer Society, Publications Board (2014 - 2015)

- Member of the IEEE Periodical Committee (PERCOM) (2014)

- Member of the IEEE Publication Services and Products Board (2014)

- Member of the CRA Committee on Education (September 2013 - 2015)

- Chair of the Search Committee for the new Editor-in-Chief of IEEE Transactions on Parallel and Distributed Processing Systems, April 2013.

- Member of the IEEE Ad Hoc Committee on Educational Activities in TA (2013)

- Member of the Program Committee of the 2013 International Workshop on Embedded Multicore Systems (ICPP-EMS 2013), organized in conjunction with the Forty Second International Conference on Parallel Processing, Lyon, France, October 1-4, 2013

- Member of the Program Committee of the Fortieth IFIP International Conference on Network and Parallel Computing (NPC 2013), Guiyang, PRC, September 19-21, 2013

- Member of a review panel for the National Science Foundation, 2013

- Vice-President and Chair, IEEE Computer Society, Educational Activities Board (2013)

- Member of the Program Committee of the *2013 International Workshop on Embedded Multicore Systems (ICPP-EMS'2013)*, Lyon, France, October 2013

- Elected member (second term) of the IEEE Computer Society Board of Governors (2013 - 2015)

- Member of three review panels for the National Science Foundation, 2012

- IEEE Computer Society Representative to the Computing Research Association (CRA) Board (January 2012 - December 2014)

- Member of the Program Committee of the Thirty Ninth IFIP International Conference on Network and Parallel Computing (NPC 2012), Gwangju, Korea, September 6-8, 2012

- IEEE Computer Society Publications Board Magazines Operation Committee Chair (2012)

- Member of the Steering Committee of the 2012 International Conference on Grid and Parallel Computing (GPC 2012), Hong Kong, May 2012

- Member of the "Future Directions in Computing" panel at 2011 International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD 2011), Vitória, Espirito Santo, Brazil, October 2011

- Member of the "Future Directions in Computing" panel at the Fourteenth IEEE International Conference on Computational Science and Engineering (CSE-2011), Dalian, PR China, August 24, 2011

- Member of a panel for the National Science Foundation, March 2011

- Member of a panel for the Department of Energy Office of Science, January 2011

- Member of a panel for the National Science Foundation, October 2010

- Member of the Program Committee of the Thirty Eighth International Symposium on Computer Architecture (ISCA '11), San Jose, CA, June 4-8, 2011

- IEEE Computer Society Publications Board Transactions Operation Committee Chair (2010 - 2011)

- Elected member (first term) of the IEEE Computer Society Board of Governors (2010 - 2012)

- Member of the IEEE Computer Society Audit Committee (since January 2010 - Chair since January 2012)

- Elected member of the IEEE Computer Society Board of Governors (2010-2012)

- Member of the Program Committee of the *2010 International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD)*, Petropolis, Brazil, October 2010

- Member of the Program Committee of the *Fifth Annual Workshop on Architectural Research Prototyping (WARP 2010)*, Rennes, France, June 2010

- Member of a panel for the Department of Energy Office of Science, May 2010

- Member of the Search Committee for the new Editor-in-Chief of IEEE Computer Architecture Letters, April 2009.

- Member of the Program Committee of the *2009 International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD)*, São Paulo, Brazil, October 2009

- Member of the Program Committee of the *Secure, Trusted, Manageable and Controllable Grid Services and Systems Workshop (STMC-Grid'2009)*, Delft, The Netherlands, August 24-25, 2009

- Member of an NSF Review panel, 2009

- Member of the Program Committee of the *2009 High Performance Computing Conference (HPC Asia 2009)*, Kaohsiung, Taiwan, March 2009

- Member of the Program Committee of the *2008 IFIP International Conference On Network and Parallel Computing (NPC 2008*, Shanghai, China, October 18-20, 2008

- Member of the Steering Committee of the *Workshop on Secure, Trusted, Manageable and Controllable Grid Services*, a workshop of the Fourteenth International Euro-Par Conference European Conference on Parallel and Distributed Computing (Euro-Par 2008), Las Palmas de Gran Canaria, Spain, August 26-29, 2008

- Member of the Program Committee of the *2008 International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD)*, Campo Grande, Brazil, October 2008

- Facilitator of an ABET session at the 2008 Annual Meeting of the Electrical and Computer Engineering Department Head Association (ECEDHA), San Diego, March 14-18, 2008

- Member of the Program Committee of the *SYMPosium en Architectures nouvelles de machines (SympA'2008)*, Fribourg, Switzerland, February 11-13, 2008

- Member of the Program Committee of the *2008 International Symposium on Frontiers in Computer Architecture Design (FCAD 2008*, National Tsing Hua University, Hsinchu, Taiwan, August 4-6, 2008

- Member of the Program Committee of the *Thirteenth Asia-Pacific Computer Systems Architecture Conference (ACSAC 2008)*, National Tsing Hua University, Hsinchu, Taiwan, August 4-6, 2008

- Member of the Program Committee of the *2008 IEEE Eleventh International Conference on Computational Science and Engineering*, São Paulo, Brazil, July 16-18, 2008

- Evaluator of the *2008 International Workshop on Ultra Low Power Data-Driven Networking Systems*, Kyoto, Japan, January 10-11, 2008

- Chair of the Panel Discussion "The Impact of MultiCore Architectures on Programming," at the *2007 International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD 2007)*, Gramado, Brazil, October 2007

- Member of the Panel Discussion "Multi-core - How can parallel computing become mainstream?," at the *IFIP International Conference on Parallel Computing Conference (NPC 2007)*, Dalian, China, September 18 - 21, 2007

- Member of the Program Committee of the Thirty Fifth International Symposium on Computer Architecture (ISCA '08), Beijing, PR China, June 21-25, 2008.

- Member of the Program Committee of the Twelfth Asia-Pacific Computer Systems Architecture Conference (ACSAC 2007), Seoul, Korea, August 23-25, 2007.

- Member of the Program Committee of the SYMPosium en Architectures nouvelles de machines (SympA'2006), Perpignan, France, October 4-6, 2006.

- Member of the Search Committee for the new Editor-in-Chief of IEEE Micro, October 2006.

- Member of the Program Committee of the IEEE 2006 John Vincent Atanasoff International Symposium on Modern Computing (JVA 2006), Sofia, Bulgaria, October 3-6, 2006.

- Member International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD) (since 2005)

- Chair of the Steering Committee of the International Conference on Parallel Architectures and Compilation Techniques (PACT) (since September 2006).

- Member of the Program Committee of the 2006 International Conference on Parallel Architectures and Compilation Techniques (PACT '06), Seattle, Washington, September 16-20, 2006

- Member of the Program Committee of the Eleventh Asia-Pacific Computer Systems Architecture Conference (ACSAC 2006), Shanghai, PRC, September 6-8, 2006.

- Member of the Program Committee of the Fifth IEEE International Symposium on Network Computing and Applications (NCA 2006), Kendall Square, Cambridge, MA, July 24 - July 26, 2006.

- Member of the Program Committee of the Twelfth International Conference on Parallel and Distributed Systems (ICPADS '06), Minneapolis, MN, July 12-15, 2006.

- Member of the Program Committee of the Thirty Third International Symposium on Computer Architecture (ISCA '06), Boston, MA, June 17-21, 2006.

- Member of the Search Committee for the new Editor-in-Chief of the IEEE Transactions on Computers, June 2006.

- Member of the Steering Committee of the Twentieth International Symposium on Parallel and Distributed Processing Systems (IPDPS 2006), Rhodes, Greece, April 2006.

- Member of the Review Committee of the "Laboratoire d'Informatique du Parallélisme," Lyon, January 9-10, 2006.

- Member of the Technical Committee on Computer Architecture Advisory Board (since July 2005).

- Member of the UCR Computer Science and Engineering Board of Advisors, 2005-2006.

- Member of the ACM/IEEE CS ad hoc committee on the Health of Conferences, 2005.

- Member of the "*Conseil de Perfectionnement du Groupe ESIEE* (Board of advisors)," 2005-2010.

- Member of the Program Committee of the 2006 International Conference on Parallel Architectures and Compilation Techniques, Seattle, WA, September 16-20, 2006.

- Member of the Program Committee of the Twelfth International Conference on Parallel and Distributed Systems, Minneapolis, Minnesota, July 2006.

- Co-chair of the Steering Committee of the IEEE/ACM International Symposium on Computer Architecture (ISCA '06), Boston, Massachusetts, June 2006.

- Member of the Steering Committee of the 2006 International Conference on Grid and Parallel Computing (GPC 2006), Taichung, Taiwan, May 2006.

- Member of the Program Committee of the Nineteenth International Conference on Architecture of Computing Systems (ARCS '06), Frankfurt, Germany, March 2006.

- Member of the Steering Committee of the IFIP International Conference on Network and Parallel Computing (NPC '05), Beijing, PRC, November 30 - December 2, 2005

- Member of the Program Committee of the Tenth Asia-Pacific Computer Systems Architecture Conference (ACSAC05), Singapore, October 2005.

- Member of the Program Committee of the IEEE International Symposium on Network Computing and Applications, (NCA05), Cambridge, Massachusetts, July 2005.

- Member of the Program Committee of the 2004 International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD), Rio de Janeiro, Brazil, October 2004

- Member of a review panel at the National Science Foundation, 2004.

- Student Travel Awards Chair for the Parallel Architectures and Compilation Techniques conference, October 2004

- Member of the Steering Committee of the IFIP International Conference on Network and Parallel Computing (NPC '04), Wuhan, P.R. China, October 18 - 20, 2004

- Member of the Program Committee of the IFIP International Conference on Network and Parallel Computing (NPC '04), Wuhan, P.R. China, October 18 - 20, 2004

- Member of the Third International Conference on Parallel Computing Systems (PCS '04) Program Committee, Colima, Mexico, September 19 - 22, 2004

- Member of the Ninth Asia-Pacific Computer Systems Architecture Conference (ACSAC '04) Program Committee, Beijing, P.R. China, September 7 - 9, 2004

- Member of the Third IEEE International Symposium on Network Computing and Applications (NCA '04) Program Committee, Cambridge, Massachussets, August 30- September 1, 2004

- Member of the Eckert-Mauchly award committee (2002 - 2003 - 2004), chair in 2003

- Member of the Steering Committee for HPCA, ISCA, PACT

- Chair of a committee within the NSF CISE Committee Of Visitors (COV), June 2003

- Member of the VUB laboratory research evaluation committee, Vrije Univ. Brussels, Belgium, October 2002

- IEEE Computer Society Technical Committee on Computer Architecture Executive Committee chair (elected June 2001 - reelected June 2003 - term ended June 2005)

- Chair of the evaluation committee of the "programme A3" at INRIA, Rocquencourt, France, October 1999

- Member of the NSF Wireless Computation program panel (June 1999).

- Member of the Advisory Board Euro-Par (1999)

- Member of the steering committee for the 1993 International Symposium on Computer Architecture

- Member of the steering committee for the SuperComputer Conference

- Core Member of the steering committee for Conference on Parallel Architectures and Compilation Techniques (PACT)

- Referee for multiple IEEE conferences, IEEE Transactions on Computers, IEEE Computer magazine, *etc.*

- Member of the *Parallel Computing* panel at the 1989 IEEE Conference on Data Engineering, Los Angeles, California, February 1989

- Session organizer at the National Computer Conference, Chicago, Illinois, June 1985 (session on *Functional Systems and Data-Flow Architectures*)

- Member of the *Parallel Computing* panel at the 1989 IEEE Conference on Data Engineering, Los Angeles, California, February 1989

- Program Committee member of ASAP '92 '93 '94 '95, CONPAR '92, Transputers '92 '93 '94 '95, FGCS '92, PARLE '93 '94, PACT '94, HPFC '95, TDP '96, PACT '98, PDSE '98, International Conference on Application of Concurrency to System Design, March 1998, Aizu Wakamatsu, Japan, PCS '99, HPCS 2003, NCA '03, *etc.*

University and Department Service at UCI

- Faculty advising session for freshmen-sophomore students, November 4, 2015

- Council on Academic Personnel Chair (September 2014 - August 2015)

- University Committee on Academic Personnel Member (September 2013 - August 2014)

- The Henry Samueli School of Engineering Executive Committee (September 2012 - present)

- Council on Academic Personnel Vice-Chair (September 2013- August 2014)

- Council on Academic Personnel, member (September 2012 - August 2013)

- The Henry Samueli School of Engineering Executive Committee on Foreign Outreach (September 2011 - Present)

- Member of the EECS Department Graduate Committee (2010 - 2011)

- EECS Department chair (January 1, 2003 - September 2, 2009)

- Chair of the School Committee on Evaluation of the ACE Program, Summer 2007

- Irvine campus representative on the Executive Advisory Committee of the Microelectronics Innovation and Computer Research Opportunities (MICRO) program, February 2007 - August 2009

- Member of the School Endowed Chairs Committee, 2006-2007

- Member of the Committee on International Education (Subcommittee of the Council on Educational Policy), 2006-2007

- Member of the HSSoE Dean Review Committee, Spring 2006

- Organizer of the 2002 Strategic Planning Department Retreat, December 2002

- Organizer of the 2002 ECE Department retreat, September 2002

University and Department Service at USC

- School of Engineering Appointments, Promotions, and Tenure Committee (chairman in 2000-2001)

- EE-Systems Department Merit review committee 1998 / 1999 (chair) /2000

- Computer Engineering Division Director (September 1998 - December 2001 - reelected in June 2001)

- Member of multiple doctoral committees

- Member of the Engineering Faculty Council (1997 - 1998)

- Ph.D. Admissions (from 1986 to 1989)

- Faculty Senate (1991-1992)

- Computer Engineering Ph.D. Screening Exam (chairman) (1991-1996)

- TA Assignments (chair) (1991-1996)

- EP&P (1991-1992)

- 1991, 1995 EE-Systems Department Merit review committee for Assistant Professors

- Computer Engineering Division Screening Exam Committee chairman (since 1991).

- Engineering Curriculum committee (Fall 1992)

- *Ad hoc* committee to review CTRF (1993)

- School of Engineering Curriculum Review Task Force (since 1994)

- EE-Systems Department Curriculum Review Task Force (since 1994)

- Promotion committees

Membership on doctoral and tenure committees outside the home university

- Member of a doctoral committee at the University de Versailles, St. Quentin-en-Yvelines, France, December 13, 2017

- Member (*Rapporteur*) of a promotion committee at the University of Paris Sud, Orsay, France, May 2013

- Member of a doctoral committee at the University of Paris Sud, Orsay, France, December 2011

- Member of a doctoral committee at the University of Lille, Lille, France, December 2011

- Member (*Rapporteur*) of a doctoral committee at the University of Paris-Est, Marne-la-Vallée, France, December 2011

- Member of a "tenure" committee at the University of Paris VII, France, December 2002

- Member of a doctoral committee at the University of Baja California, Ensenada, Mexico, May 2002

- Member of a doctoral committee at the University of Joensuu, Finland, April 2002

- Member of a doctoral committee at the "Universidade de São Paulo," São Paulo, Brazil, October 2001

- Member of a "tenure" committee at the University of Rennes, Rennes, France, September 2000

- Member of a doctoral committee at the University of Rennes, Rennes, France, February 2000

- Member of a "tenure" committee at the Université Paris VII, Paris, France, December 1999.

- Member of a "tenure" committee at Vrije Univ. Brussels, Belgium, May 1999

- Member of a doctoral committee at the *École Nationale Supérieure des Télécommunications,* Paris, France, March 1999

- Member of a doctoral committee at the University of Rennes, Rennes, France, October 1998

- Member of a doctoral committee at the Université Paris VI, Paris, France, May 1998

- Member of a doctoral committee at Bridgewater State College, Massachusetts, December 1997

Invitations and collaboration with other research groups

- *Université de Paris Est,* Marne-la-Vallée, France, September 2017.

- *Université de Paris XIII,* Paris, France, September-October 2016.

- *Academia Sinica*, Taipei, Taiwan, September 4-9, 2016.

- *Nagoya Institute of Technology,* Nagoya, Japan, August-September, 2016.

- *Institut Eurecom,* Sophia Antipolis, France, June 2010.

- *INRIA,* Rocquencourt, France, April - June 2010.

- *CICESE,* Ensenada, Mexico, several visits since 2000.

- *INRIA,* Rocquencourt, France, multiple visits since 1997, including 1 month in November 1997.

- *Ecole Nationale Supérieure des Télécommunications,* Paris, France, July - December 1997.

- *Université de Picardie, Amiens,* France, June 1997.

- *Ecole Nationale Supérieure des Télécommunications,* Paris, France, May-July 1994.

- *Ecole Supérieure d'Ingénieurs en Electrotechnique et Electronique,* Paris, France, December 1990: research on parallel architectures for image processing.

- *Royal Melbourne Institute of Technology,* Melbourne, Australia, December 6, 1988 through January 10, 1989: research on the RMIT data-flow project.

- *NTT Musashino Research Center,* Tokyo, Japan, June 1989.

- *Ecole Supérieure d'Ingénieurs en Electronique et Electrotechnique,* Paris, France, July 1988.

September 11, 2018